EXHIBIT 2

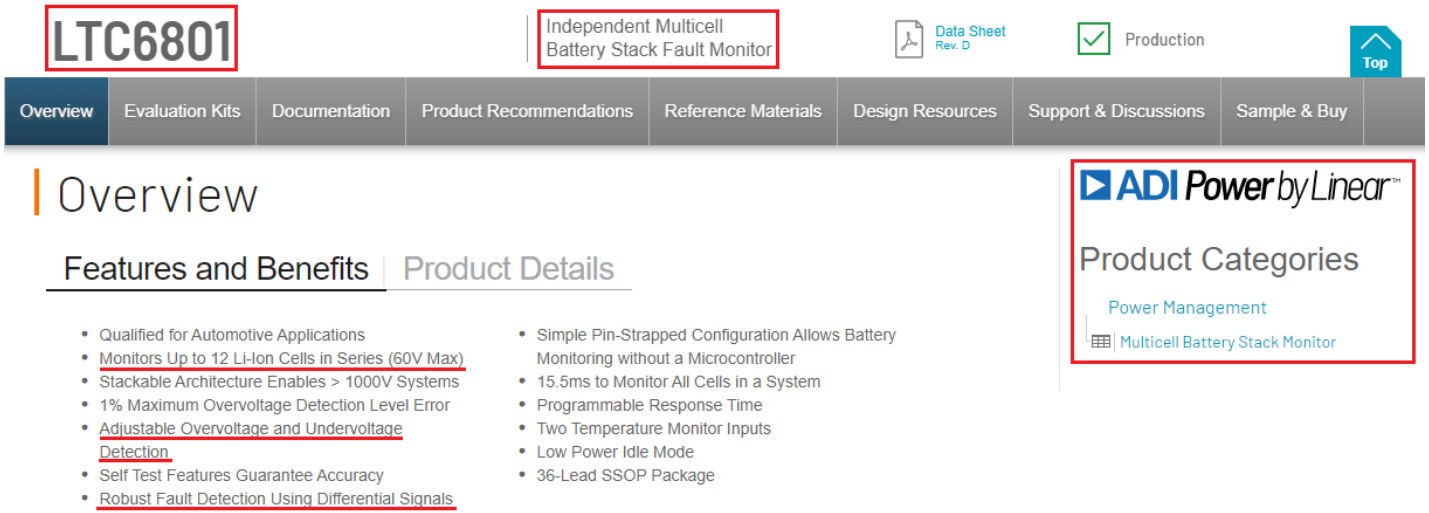
US6346795	Analog Devices 'LTC6801' ("The accused product")
1. A discharge control circuit for controlling discharge of a battery including at least one cell comprising:	The accused product comprises a discharge control (e.g., Undervoltage detection circuit) circuit for controlling discharge of a battery (e.g., cells of battery) including at least one cell.  https://www.analog.com/en/products/ltc6801.html?doc=LTC6801.pdf#product-overview

EXHIBIT 2

ANALOG DEVICES

LTC6801

Independent Multicell Battery Stack Fault Monitor

FEATURES

- **Qualified for Automotive Applications**
- **Monitors Up to 12 Li-Ion Cells in Series (60V Max)**
- **Stackable Architecture Enables >1000V Systems**
- **1% Maximum Overvoltage Detection Level Error**
- **Adjustable Overvoltage and Undervoltage Detection**
- **Self Test Features Guarantee Accuracy**
- **Robust Fault Detection Using Differential Signals**
- Simple Pin-Strapped Configuration Allows Battery Monitoring without a Microcontroller
- 15.5ms to Monitor All Cells in a System
- Programmable Response Time
- Two Temperature Monitor Inputs
- Low Power Idle Mode
- 36-Lead SSOP Package

APPLICATIONS

- Redundant Battery Monitor
- Hybrid Electric Vehicles

DESCRIPTION

The LTC®6801 is a multicell battery monitoring IC incorporating a 12-bit ADC, a precision voltage reference, sampled comparator, and a high voltage input multiplexer. The LTC6801 can monitor as many as 12 series connected battery cells for overvoltage, undervoltage, and overtemperature conditions, indicating whether the cells are within specified parameters. The LTC6801 generates a clock output when no fault conditions exist. Differential clocking provides high noise immunity and ensures that battery stack fault conditions cannot be hidden by frozen bits or short circuit conditions.

Each LTC6801 can operate with a battery stack voltage up to 60V and multiple LTC6801 devices can be stacked to monitor each individual cell in a long battery string. When multiple devices are stacked, the status signal of each LTC6801 can be daisy-chained, without opto-couplers or isolators, providing a single status output for the entire battery string.

https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6801.pdf

EXHIBIT 2

Table 2. Undervoltage Inputs

UV1	UV0	UNDERVOLTAGE THRESHOLD (V)
V_{REG}	V_{REG}	2.871
V_{REG}	V_{REF}	2.680
V_{REG}	V^-	2.489
V_{REF}	V_{REG}	2.297
V_{REF}	V_{REF}	2.106
V_{REF}	V^-	1.914
V^-	V_{REG}	1.723
V^-	V_{REF}	1.531
V^-	V^-	0.766

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EXHIBIT 2

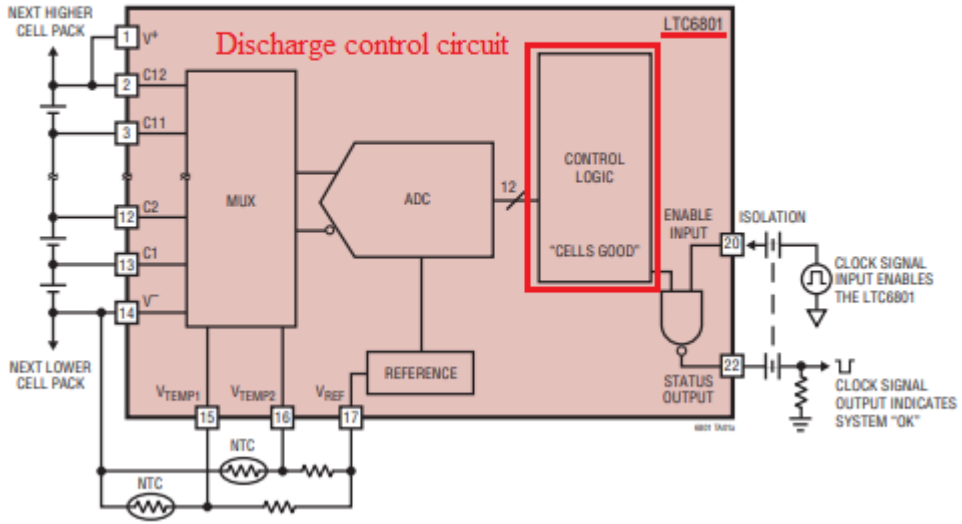
	BLOCK DIAGRAM  https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6801.pdf
a discharge control switch connected to the battery for cutting off a discharge current of the battery in response to a discharge stop signal; and	The accused product comprises a discharge control switch connected to the battery for cutting off a discharge current (e.g., turning off switch) of the battery in response to a discharge stop signal (e.g., UV control signal provided by the control circuit).

EXHIBIT 2

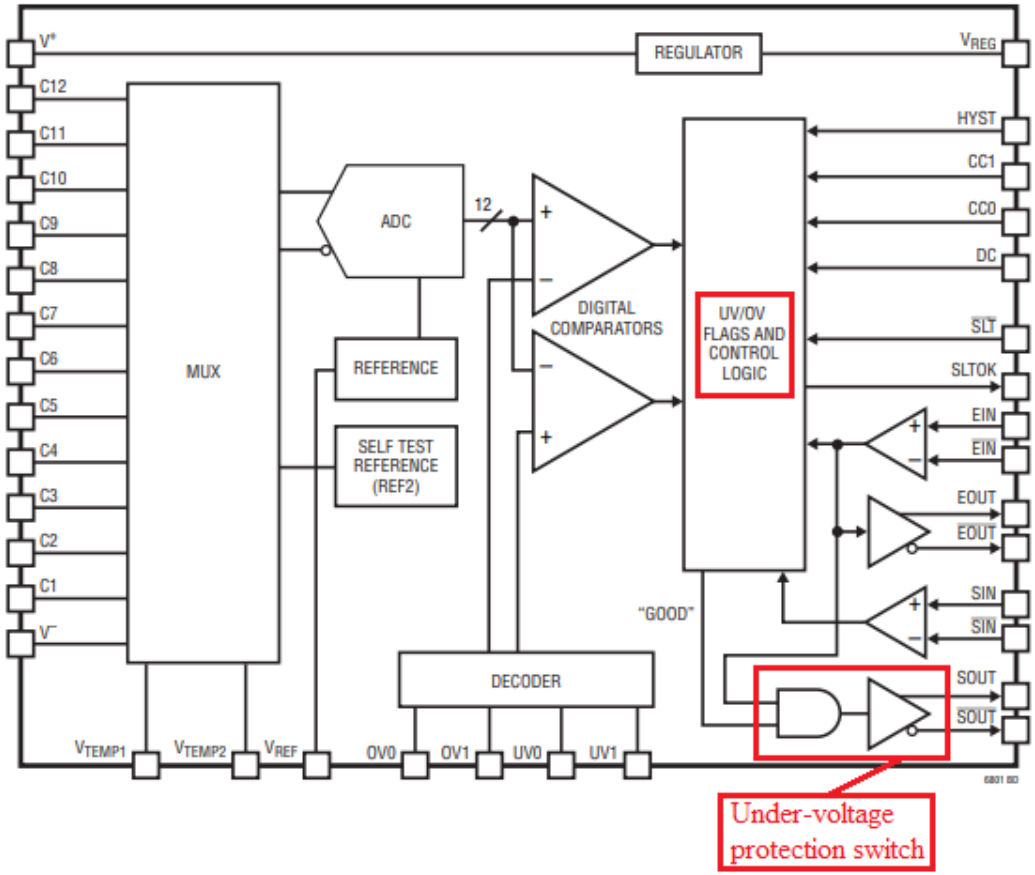


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EXHIBIT 2

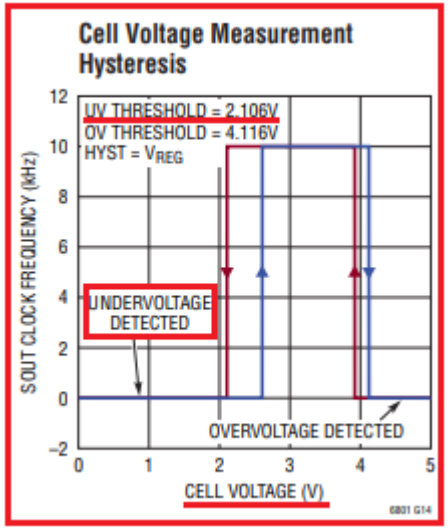
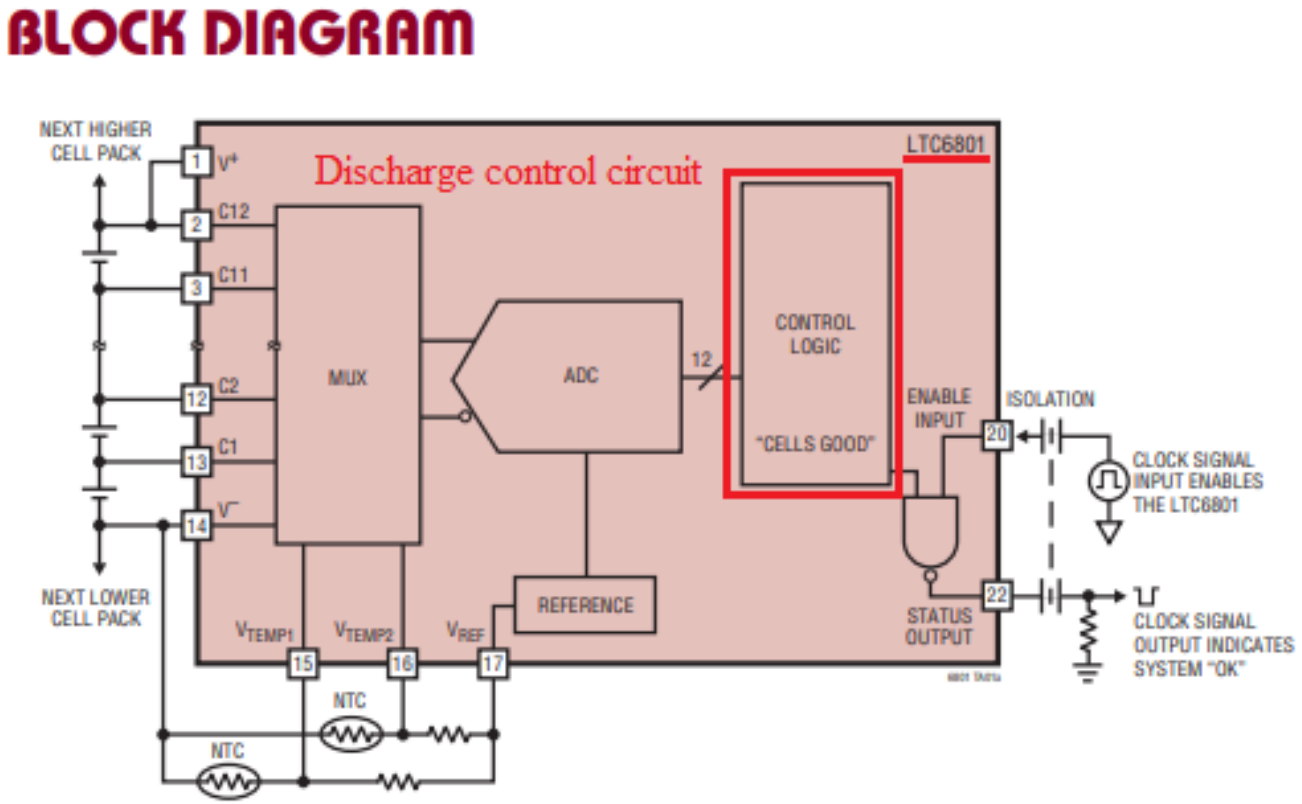
	 https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6801.pdf
a control circuit connected to the battery and the discharge control switch for generating -the discharge stop signal that deactivates the discharge control switch when a voltage of at least one cell reaches a lower limit, wherein the control circuit	The accused product comprises a control circuit connected to the battery and the discharge control switch for generating the discharge stop signal (e.g., undervoltage signal provided by the control circuit) that deactivates the discharge control switch when a voltage of at least one cell reaches a lower limit (e.g., UV Threshold Voltage), wherein the control circuit includes a switch holding circuit (e.g., delay generating circuit) for continuously supplying the discharge stop signal to the discharge control switch for a predetermined time (e.g., delay time set by the circuit) after the discharge stop signal is generated.

EXHIBIT 2

includes a switch holding circuit for continuously supplying the discharge stop signal to the discharge control switch for a predetermined time after the discharge stop signal is generated.	 https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6801.pdf

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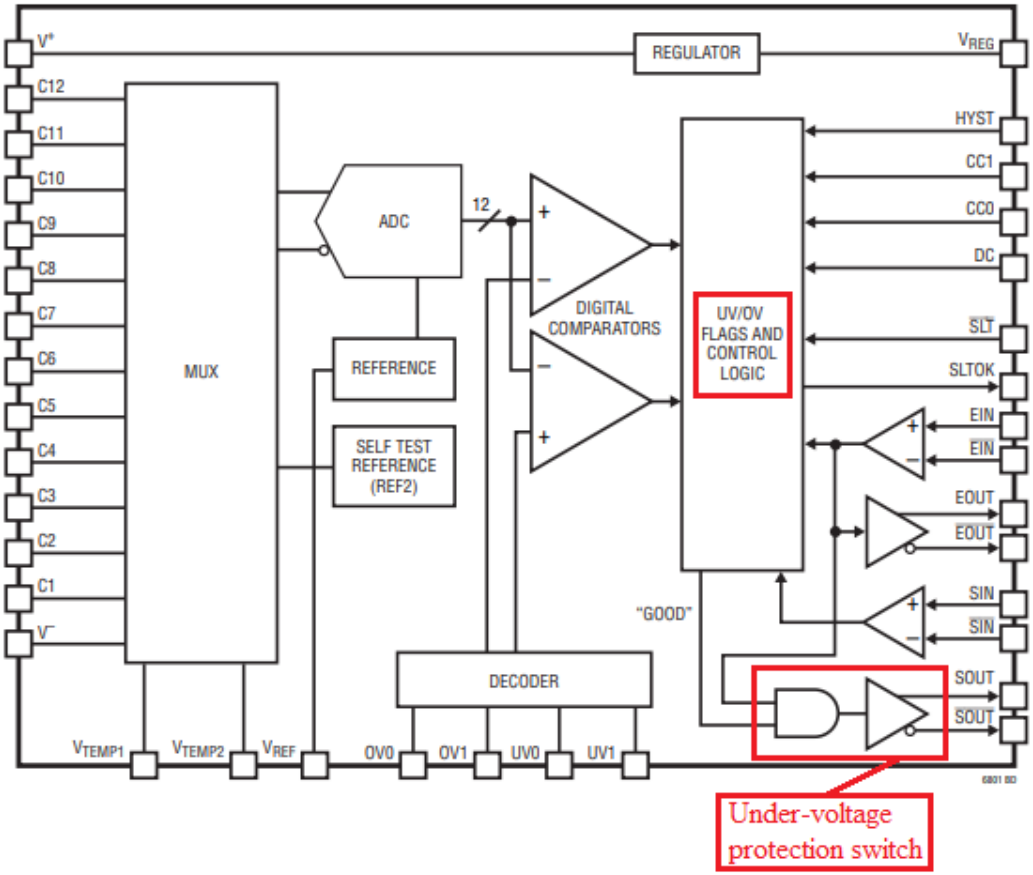

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	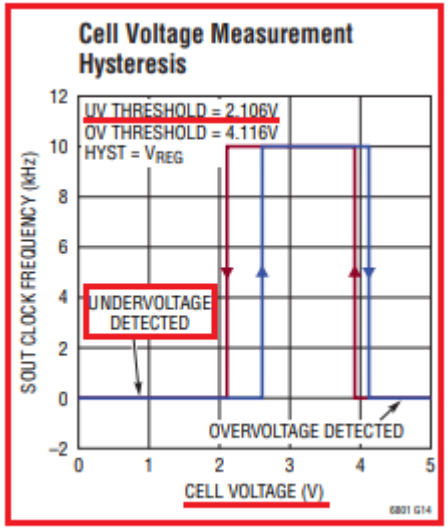 https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6801.pdf

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EXHIBIT 2

The maximum delay between when a bad cell voltage occurs and when it is detected depends on the measurement duty cycle setting. The SOUT clock turns on or off at the end of each measurement cycle. Figure 4 shows the maximum detection delay in continuous monitor mode (DC pin tied to V_{REG}).

Note: If an internal self test occurs immediately after the fault, the maximum detection delay will be increased by an additional measurement cycle time.

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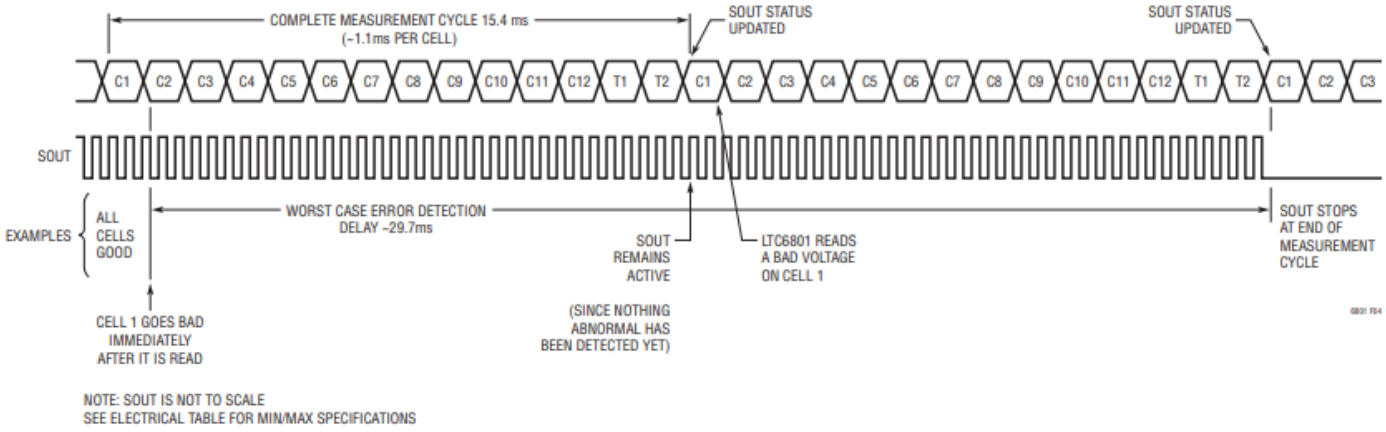

Figure 4. Cell UV/OV Detection Delay in Continuous Monitor Mode

https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6801.pdf